REMARKS

Claims 1, 2 and 4 through 23 are pending in this application. Claims 1, 7, and 15 are the independent claims. Claims 1, 7 and 15 have been amended. Claim 3 has been withdrawn without prejudice or disclaimer of the subject matter therein.

The Examiner has objected to Fig. 1 of the drawings due to minor informalities. Specifically, the Examiner has required component 140 in Fig. 1 to be labeled as a 64-bit address register for further clarity. The Examiner has objected to claim 18 due to minor claim informalities. The Examiner has rejected claims 1 through 23 under 35 U.S.C. § 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992.

IN THE DRAWINGS

The Examiner's objections to the drawings are acknowledged and filed concurrently herewith is a Letter to the Official Draftsperson in which a red-lined copy of the originally filed drawing indicating the required correction to label component 140 in Fig. 1 as a "64-bit ADDRESS REGISTER" is submitted for the Examiner's review and approval.

No new matter has been added to the drawings and all corrections are fully supported by the specification. Corrected final drawings are being prepared and will be filed upon receipt of the Examiner's approval of the revised drawings.

CLAIM OBJECTIONS

The Examiner has objected to claim 18 due to minor claim informalities. Claim 18 has been amended to incorporate the Examiner's suggested correction to overcome the objection. Therefore, Applicants believe the above amendment has rendered the objection moot and respectfully request the objection be withdrawn.

REJECTIONS UNDER 35 U.S.C. § 102

The Examiner has rejected claims 1 through 23 under 35 U.S.C. § 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992. Referring to claim 1, the Examiner states that Killian has taught a processor comprising:

"(a) means for executing an instruction of an application of a first bit size

ported to a second bit size environment, the second bit size being greater than the first bit size. See column 2, lines 7-33.
(b) means for confining the application to a first bit size address space subset (see column 19, lines 36-40), said means for confining comprising:
(i) means for truncating generated address references of the second bit size to the first bit size. See column 10, line 62, to column 11, line 5. In this passage the Examiner states that Killian explains that the 32-bit architecture ignores overflow (i.e., performs truncation) during addition operations. The Examiner alleges that since Killian's system is backward compatible with the aforementioned 32-bit architecture, it follows that Killian's system would perform the same operations as the 32-bit architecture. Therefore, in overflow situations, truncation would be performed on 64-bit data (since the data path and register size of Killian's system is 64-bits) in order to obtain 32-bit data.
(ii) means for extending to the second bit size the truncated generated address references based at least in part on a setting of a predetermined control signal. See column 12, lines 45-65, and column 17, lines 27-31. The Examiner notes that 32-bit data is sign extended for use in the extended architecture. The Examiner further notes that if the particular status register bits (predetermined control signal) specifies 32-bit mode, the addresses are sign-extended from 32 bits to 64 bits. In 64-bit mode, no sign extension occurs.

In response to Applicant's arguments filed on April 14, 2003, the Examiner states, *inter alia*:

". . . While the Applicant may be correct in arguing that the "address format control flag" taught by Killian et al. Is more accurately analogized to the address space control flag, the "address format control flag" of Killian et al. still results in 32-bit references being extended to 64-bits. Although Applicant's [sic] address format control flag determines whether to zero-extend or sign-extend a 32-bit value, the absence of limitation in claim 1 allows for anticipation by Killian et al." (See Office Action, pages 10 through 11, paragraph 32.)

Claim 1 has been amended to recite, *inter alia*:

"means for extending to the second bit size the truncated generated address references based at least in part on a setting of an address format control signal, the setting of the address format control signal to determine whether the truncated generated address references are to be zero-extended or sign-extended."

Since the Examiner agrees with Applicants that the Killian et al. "address format control flag," now "address format control signal", is more accurately analogized to the "address space control flag," it therefore does <u>not</u> or is not used to determine

"whether the truncated generated address references are to be zero-extended or sign-extended," as recited in claim 1. Indeed, there is no equivalent structure in Killian et al. that is used to explicitly specify whether the truncated 32-bit addresses are to be zero-extended or sign-extended. Therefore, Applicants believe the above amendments have rendered the rejection moot and respectfully request the Section 102 rejection of claim 1, and the claims that depend therefrom, be withdrawn.

Claims 7 and 15 have been similarly amended to recite, *inter alia*: "extend(ing) the truncated, generated address reference from the first bit size to the second bit size based at least in part on a setting of an address format control signal, the setting being used to determine whether to zero-extend or sign-extend the truncated generated address references." For at least those reasons given above for claim 1, Applicants believe the above amendments have rendered the rejection of claims 7 and 15, and the claims that depend variously therefrom, moot and respectfully request the Section 102 rejection be withdrawn.

Accordingly, Applicants believe that claims 1, 2 and 4 through 23 are allowable over the applied art and respectfully request a notice of allowance to that effect be issued.

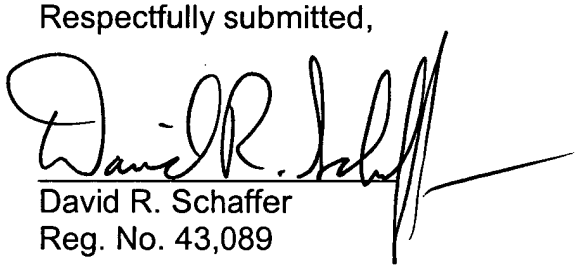
CONCLUSION

In view of the above remarks, the Applicants respectfully submit that the present case is in condition for allowance and request the Examiner issue a notice of allowance to that effect.

The Commissioner is hereby authorized to charge any additional fees required under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to **Deposit Account No. 11-0600**.

The Examiner is invited to contact the undersigned at (202) 220-4263 to discuss any matter concerning this application.

Respectfully submitted,



Dated: July 11, 2003

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